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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,643	11/24/2003	Richard M. Fastow	AMD-H0564	7105

7590 09/07/2004

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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,643	FASTOW ET AL.	
	Examiner	Art Unit	
	Pho M Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-21* is/are allowed.

6)☒ Claim(s) *1,2,4 and 7* is/are rejected.

7)☒ Claim(s) *3,5,6 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Drawings

1. The drawings are objected to because of the hand drawing. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1-2, 4 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Nair et al. (US. 6,529,398).

Regarding claim 1, Nair et al. In Figure 2 and Figures 4-5 disclosed a method for reading a flash memory cell (memory device 40 including memory array 42 having bit lines 48 and word line 46 and flash memory cell 10 in Figure. 2) comprising:

accessing leakage current (active bit line ABL 22 to receive the current I_{BL_DAT} which includes a signal current applied to integrating amplifier 118 included of an operational amplifier 119 in Figure. 4) of a common bit line in the flash memory cell (memory cell 10 having word line 46 and bit line 48 in Figure. 2);

accessing read current (reference bit line RBL 122 to receive the current I_{BL-REF}) of the flash memory cell (memory cell 10, Figure. 2);

eliminating the leakage current form the read current (the actual signal and current charge provided by the substrate an current obtained from a reference bit line RBL 122 with current I_{BL-REF} and active bit line ABL 122 with current I_{BL-DAT} in Figure 5) to determine a cell current (the cell current with the combine of ABL and RBL in Figure 5); and

comparing the cell current to a verify cell current (the actual signal input in combine of ABL and RBL; and input of V_{REF} 119 in Figure 5 get output signal OUTPUT A for verified cell current).

With respected to claim 2, Nair et al. in Figure 5 disclosed a method for reading a flash memory cell comprising the verify cell is a read (the input in combine of ABL, RBL and input VREF, both input have current store at operation amplifier 119 corresponding to the output (OUTPUT A) for verified cell is a read current cell) verify cell.

With respected to claim 4, Nair et al. in Figure 2 disclosed a method for reading a flash memory cell which is the flash memory cell (10) is disposed in an array of flash memory cells (memory array 42), the cell arranged with at least one common word line (word line 48) and one common bit line (bit line 46).

With respected to claim 7, Nair et al. in Figure 5 disclosed a method for reading a flash memory cell which is the eliminating the leakage current from the read current comprises subtracted a voltage (ABL and RBL having voltage applied to operation amplifier 119 which is the provide by the substrate an current obtained from a reference

bit line RBL (read current) and active bit line ABL (leakage current)) corresponding to the read current from a voltage corresponding to the leakage current.

Allowable Subject Matter

4. Claims 3, 5-6, 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 3, the prior art of record do not disclose or suggest a method for reading a flash memory cell which is the verify cell is an erase verify cell.

Regarding claim 5, the prior art of record do not disclose or suggest a flash memory cell for a read operation with a control gate voltage at approximately zero volts.

Regarding claim 8, the prior art of record do not disclose or suggest the voltage corresponding to the leakage current is stored on a capacitive element.

Regarding claim 9, the prior art of record do not disclose or suggest the flash memory cell which the floating gate as a storage element.

Regarding claim 10, the prior art of record do not disclose or suggest the flash memory cell which a nitride layer as a storage element.

6. Claims 11-21 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "applying an erase pulse to the sector of flash memory to performing a method for verifying erasure of each flash memory cell in the sector of flash memory" as claimed in the independent claim 11; or

"the third circuit for eliminating the leakage current from the read current to determined a cell current that coupled to the first circuitry and second circuitry" as claimed in the independent claim 17.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kurihara et al. (US. 6,525,969) disclosed a memory cell is selected to read and an adjacent memory cell is pre-charged to mitigate leakage current associated with the cell.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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2 September 2004

Pho M. Luu
Patent Examiner
Art Unit 2824